

### **REMARKS/ARGUMENTS**

Claims 46, 50, and 51 are amended to correct typographical errors (not for reasons of patentability). Claims 46-57 remain pending in the application. Applicants respectfully request reexamination and reconsideration of the application.

Claims 46-55 were rejected under 35 USC § 112, first paragraph. Claims 46, 50, and 51 are amended to correct typographical errors, which should moot this rejection.

Claims 46-57 were rejected under 35 USC § 102(b) as anticipated by US Patent No. 5,070,297 to Kwon et al. ("Kwon"). Applicants respectfully traverse this rejection.

As correctly noted in the Office Action, the claims at issue are product-by-process claims. As set forth in the MPEP, "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. . . . If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." (MPEP § 2113 (quoting *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).) "Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art." (MPEP § 2113.)

In accordance with the foregoing procedure, Applicants assert that the use of the blade on the contact structure of each of the claims in the present application will result in smaller gouge marks on the bond pads of the semiconductor device of the present claims than the gouge marks that will be created by Kwon's probes 16 on the pads 19 of the IC chip. Moreover, Applicants assert that this difference—smaller gouge marks on bond pads—is an advantageous and patentable difference.

More specifically, as is known in the industry, a semiconductor die is tested by bringing probes into contact with bond pads on the die. Such probes are typically designed to wipe across the bond pads to cut through oxide or other contaminants on the bond pads and thereby create a low resistance electrical connection with the bond pads. The wiping motion of the probes creates gouge marks on the bond pads, and as is also known in the industry, such gouge marks have at least three potentially detrimental effects. First, gouge marks may prevent a wire from being bonded to a bond pad. (The bond pads of a die are often connected to a die package by wires.)

Second, even if a wire is successfully bonded to a bond pad, a gouge mark may decrease the effective life of the bond between the wire and the bond pad. Third, a gouge mark may weaken a bond pad, causing the bond pad to loosen or even detach from a die. (See U.S. Patent No. 5,506,499 to Puar ("Puar"), col. 2, lines 21-40 and col. 3, lines 7-25. Applicants assume that the Examiner can readily obtain a copy of Puar, but Applicants will provide a copy of Puar upon request.) The larger the gouge mark on a bond pad, the more pronounced the foregoing detrimental effects are likely to be. It should be apparent therefore that reducing the size of the gouge marks on bond pads of a semiconductor die represents a desirable improvement.

Each of the claims at issue wipes "tip structures" of a probe card assembly or interface board across "electrical contact terminals" of a semiconductor device. Each tip structure includes a blade oriented within about 45 degrees of, within about 30 degrees of, within about 15 degrees of, or "substantially" parallel to a wiping action of the tip structure. As described in the specification, the blade slices or cuts cleanly through any oxide or contaminant on the electrical contact terminals of the semiconductor device. (See, e.g., pg. 10, lines 18-23 and pg. 11, line 8 through pg. 12, line 4.) The clean slicing action of the blade of the claims at issue results in a smaller gouge mark than the gouge marks that are made by the conventional probes like 16 of Kwon. Indeed, US Patent No. 6,759,858 to Roggel ("Roggel") describes the gouge mark created by a blade as "small." (Roggel col. 3, lines 64-65.) (Applicants note that Roggel, whose filing date is October 20, 1999, is not prior art to the present application, whose priority date is November 10, 1998.)

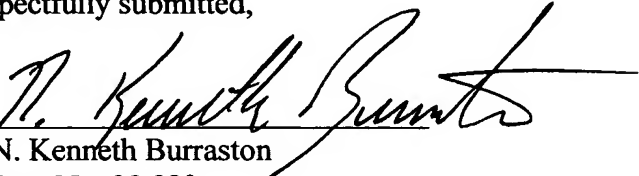
Applicants have thus "come forward with evidence establishing an unobvious difference between the claimed product and the prior art." (MPEP § 2113.) Namely, the tested semiconductor device of the claims of the present application have smaller gouge marks on their contact terminals than Kwon's IC chip. Indeed, Kwon says nothing about reducing the size of the gauge marks on pads 19. In fact, Kwon teaches making probe tips 18 of a hard material to ensure that the tips 18 penetrate contaminants on the pads 19. (Kwon col. 4, lines 60-64.) Thus, if anything, Kwon encourages increasing—not decreasing—the size of the gauge marks. Kwon therefore neither anticipates nor renders obvious the claims of the instant application.

In view of the foregoing, Applicants submit that all of the claims are allowable and the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (801) 323-5934.

Respectfully submitted,

Date: June 17, 2005

By

  
N. Kenneth Burraston  
Reg. No. 39,923

Kirton & McConkie  
1800 Eagle Gate Tower  
60 East South Temple  
P.O. Box 45120  
Salt Lake City, Utah 84111-1004  
Telephone: (801) 323-5934  
Fax: (801) 321-4893